UNITED STATES PATENT APPLICATION

FOR

METHOD AND SYSTEM FOR HIGH SPEED USB DATA ROUTING

Inventor(s):
Mahesh SIDDAPPA

Sawyer Law Group LLP
2465 E. Bayshore Road, Suite 406
Palo Alto, California 94303

METHOD AND SYSTEM FOR HIGH SPEED USB DATA ROUTING

FIELD OF THE INVENTION

The present invention relates to routing of USB data streams, and more particularly to serial data routing of high speed USB data streams.

BACKGROUND OF THE INVENTION

The Universal Serial Bus (USB) is a peripheral bus specification developed by PC and telecom industry leaders. USB Specification version 1.1 supports two different rates for transmitting data: 1.5 Mega bits (Mbits) per second for low-speed devices and 12 Mbits/second for full speed devices. Recently a USB Specification Version 2.0 was made available. USB Specification 2.0 extends the rate for transferring data from 12 Mbps (referred to herein as 12MHz) on USB 1.1 up to 480 Mbps (referred to herein as 480MHz) on USB 2.0 for high speed devices.

Under the specification, the USB allows the plug-and-play capability of computer peripherals outside the PC case. The capability eliminates the need to install interface cards into dedicated computer slots and reconfigure the system each time a peripheral is attached or detached from a PC. Typically, a USB system may be expanded by providing a USB hub which provides USB port replication. A USB hub may be connected to another USB hub and service multiple USB ports. Up to 127 devices may be connected to a data processing system through a USB interface.

As shown in an example in FIG. 1, a host 12, i.e. a computer system, includes ports 1, 2 that provide USB connection points to devices 14 and a USB hub 16. Under the

protocol of USB standard, devices 14 are classified into mainly three types. The first one is the type of a human-interface device (HID), i.e. keyboard, mouse, or, alternately, an interrupt device. The second one is the type of a bulk device, i.e. a scanner, which places strict requirement on accuracy of each data bits transmitted. The third one is the type of an isochronous device, i.e. an audio device, which does not place strict requirement on accuracy of each data bits transmitted. As indicated, the hub 16 is a device which provides additional attachment points for the host 12 to devices 14.

Hub 16 is therefore a key element in the plug-and-play architecture of computer system 12, and is a wiring concentrator which enables the multiple attachment characteristics of USB. The upstream port of hub 16 connects the hub 16 towards the host 12. Each of the downstream ports of hub 16 allows connection to another hub or device 14. Hub 16 detects the attachment and detachment of a USB device 14 at each downstream port and enables the distribution of power to these downstream USB devices 14.

In routing the data within the hub 16, complexity is increased at the high speed operation of 480MHz under USB 2.0. While attempts to reduce the frequency during the routing have been made, such attempts have their own complexities due to synchronization, timing, and clocking issues during conversion of the frequency to a lower frequency for routing from the source port and then back to a higher frequency at the destination port. Accordingly, a need exists for a routing scheme for USB connections that supports high speed operation efficiently and effectively. The present invention addresses such a need.

SUMMARY OF THE INVENTION

Aspects for high speed USB data routing are presented. The aspects include routing a data stream to and from USB I/O ports serially, and maintaining a frequency of the data stream during the routing. Additionally, a root port router is provided for the root port and a data port router is provided for each I/O port, wherein each data port router delays the data stream by one bit during the routing.

Through the present invention, an effective and straightforward routing solution for USB data transfers at high speed is achieved. The present invention utilizes a serial data routing scheme that is less complex when compared to parallel routing solutions which rely on data conversions to lower speeds during routing. These and other advantages of the present invention will be more fully understood in conjunction with the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a block diagram representation of a typical computer system with USB connections.

Figure 2 illustrates a router portion of a USB hub in accordance with a preferred embodiment of the present invention.

Figure 3 illustrates a more detailed representation of the routers of Figure 2.

Figure 4 illustrates signals transmitted within the router portion of Figure 2.

DETAILED DESCRIPTION

The present invention relates to data routing of high speed USB data. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

The present invention provides data routing of data streams between USB connections utilizing a serial routing scheme. Figure 2 illustrates an overall block diagram of a router portion of a USB hub implementing the serial routing scheme of the present invention. It should be appreciated that although the description of the aspects of the present invention is presented with reference to implementation in a USB hub, this is meant as illustrative and not restrictive of an environment within which the present invention finds particular benefit.

Referring to Figure 2, a router portion of a USB hub is shown as an example of a preferred embodiment of the present invention and includes a root port 20 (Port0) and four I/O (input/output) ports 22 (Port1, Port2, Port3, and Port4), each of which includes data buffers. Although only four I/O ports are illustrated, the present invention may be implemented with a different number of I/O ports, as needed. However, the serial routing scheme of the present invention introduces a delay of one clock between the I/O ports, so that, under the USB specification at the time of the invention, the total number of I/O ports is limited to no more than seven.

Referring again to Fig. 2, coupled to the root port 20 is a root port router 24. Coupled to each I/O port 22 is a data port router 26. The data port routers 26 are coupled in series one to another with the data port router 26 of Port1 coupled in series with the root port router 24. The root port router 24 is further coupled to a high speed serial interface engine 28 (HS SIE), which performs preprocessing including enumeration of the circuit and the resetting and enabling of each I/O port 22, as is well appreciated by those skilled in the art. Coupled to each data port router 26 is a data port control block 30 which provides signals for I/O port enabling, as illustrated more particularly with reference to Figure 3.

Figure 3 illustrates a more detailed diagram of the router portion shown in Figure 2. The data port routers 26 each contain the same elements. Thus, within each data port router 26 are delay elements 32a, 32b, 32c, 32d (e.g., flip/flops) and a selection element 34 (e.g., a multiplexer). Two two-bit wires are input to each I/O port 22 from its corresponding router 26 and one two-bit wire is output from each I/O port 22 to its corresponding router 26. All of the connections to and from the root router 24 and at least one of the data port routers 26 carry signals at a frequency of 480MHz. Further, each two-bit wire carries an enable signal and a data signal, such that every bit of a data stream has an enable bit. HS1 represents a high speed input for the data stream to the I/O port 22. HS2 represents a high speed input for auto-negotiation data (i.e., "CHIRP" data) from the data control block 30 to the I/O port 22.

During routing, data is sent serially one bit at a time downstream from the root port router 24 through the data port routers 26. Delay element 32a in each data port router 26 provides a one-bit delay as the data stream is transmitted from router to router downstream. Each data port control block 30 supplies a PORT ENABLE for CONNECTIVITY signal to

each router 26 for its corresponding I/O port 22 in order to enable or disable the port 22 for receipt of the data stream. Regardless of whether the port 22 is enabled or disabled, the data stream is still transmitted through each router 26. In the upstream direction, data from one of the I/O ports 22 is routed through the selection element 34 and delay element 32b of each data port router 26 to the root port router 24. The root port router selection element 36 controls whether the upstream data is passed or a new high speed data stream is passed to the root port 20 to avoid data collision. Bias 38 and termination 40 represent circuit elements necessary to meet USB specifications, the details of which are well understood in the art. Delay elements 42a, 42b, 42c, and 42d are also included in the root port router 24.

Figure 4 illustrates more particularly signal lines present between the root port router 24 and I/O port router 26 for Port1 in accordance with the serial data routing of the present invention. The names on the signal lines are meant as illustrative of the information transmitted on the signal lines, where "up" is port[i] to port[i-1], "dn" is port [i] to port[i+1], "tx" is for the outputs of the module, "SOF" is start of frame, RouterEN is router enable, and "Disc" is disconnect. The Disc signal checks for disconnect of a downstream device at a particular time in the USB frame. In the USB 2.0 specification, there are eight micro-frames within one millisecond period during the HS modes of operation. The signal Eof2Time refers to a particular time stamp inside the micro-frame. It is a defined USB frame time stamp to check for proper operation of down stream devices. As demonstrated by this figure, the data routing in accordance with the present invention utilizes a minimal number of signal lines in a straightforward and relatively uncomplicated manner.

Thus, the present invention achieves an effective routing solution for USB data transfers at high speed that avoids the complexity of layout, timing, clock skew, and physical

implementation limitations of typical parallel routing solutions which rely on data conversions to lower speeds during routing. Further, the serial routing scheme offers consistency among the routers in a manner that provides greater flexibility for adjusting to the number of I/O ports being used.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.